DYNAMIC POWER MANAGEMENT OF SOLID STATE MEMORIES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to memory controllers for solid state memories and particularly to such a memory controller having a power management function allowing the power consumption of solid state memories to be curtailed.

State of the Art

One of the present trends in computing is toward increasing miniaturization. Laptop, notebook and palmtop computers represent the fastest growing market segment in the computer market. Particularly with regard to laptop and notebook computers, the demand for mass storage devices for such computers, coupled with the space constraints inherent in building these machines, has resulted in the form factor of disk drives being driven from 5¼ inch to 3½ inch and now down to 2½ inch. The projected trend is from

2½ inch form factor drives prevalent today toward sub-two-inch drives in 1994 and sub-one-inch drives in 1997.

As the form factor of disk drives becomes smaller, a multitude of serious problems may be expected to be encountered. Small disk plating techniques exhibit very low production yields. Since very low flying heads or even contact recording heads are required due to low linear disk speed and higher bit densities, contact of the head with the disk can cause "head slapping", resulting in higher shock requirements and excessive disk wear. Low-yield thin-film heads or vertical recording technology heads are required, as are small bearings or ceramics for the necessary motors and actuators. Signals-to-noise ratios will be significantly decreased, forcing the user to tolerate higher error rates and possible data loss. To accentuate the foregoing difficulties, hard disk suppliers are becoming fewer. As a result, the magnetic hard disk found in high-volume notebook PCs is expected to become difficult to purchase due to difficulty on the part of the hard disk manufacturer of supplying quality merchandise that can be produced with economical yields.

In contrast to the foregoing situation, solid state semiconductor memories, in particular DRAMs, are presently in abundant supply at relatively low cost. In

this respect, DRAMs represent an attractive alternative to small form factor disk drives for mass memory storage. Unfortunately, however, DRAMs continually consume power, a scarce commodity in notebook applications. What is needed then is a way of curtailing the power consumption of DRAMs so that they may be used for mass memory storage in notebook applications. Using DRAMs, memory performance may be increased by a factor of several times over comparable hard drives.

SUMMARY OF THE INVENTION

According to the present invention, a dynamic power management device for supplying power to a solid state memory integrated circuit includes power control circuitry for supplying a variable voltage to the memory integrated circuit and logic control circuitry responsive to data access activity for generating address and control signals for the memory integrated circuit and for controlling the power control circuitry to supply power to the memory integrated circuit sufficient to maintain memory information in the memory integrated circuit during periods of no data access activity and sufficient to exchange memory information with the memory integrated circuit

during periods of data access activity. Power consumption of the memory integrated circuit is thereby curtailed.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be further understood from the following detailed description in conjunction with the appended drawings. In the drawings:

Figure 1 is a block diagram of the dynamic power management device of the present invention;

Figures 2a, 2b, 2c and 2d are ~~Figure 2, including Figures 2a-2d, is a~~ waveform ~~diagram~~ diagrams illustrating variable voltage control during DRAM operation;

Figure 3 is a block diagram illustrating how multiple dynamic power management devices may be daisy chained together;

Figure 4 is a waveform diagram of the voltage across string of four DRAMs during dynamic power management;

Figure 5 is a graph of the power consumption of the four DRAMs;

Figure 6 is a graph showing the cumulative amount of battery power consumed by the four DRAMs; and

Figure 7 is a graph of expected battery life over time as a function of power consumption.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The dynamic power management device implements a dynamic power management strategy having several different elements in order to achieve significant power savings. Dynamic power management is applied not only to solid state memories but also to the dynamic power management device itself. The basic element of the power conservation strategy is to essentially turn off all functions not required at any particular time. The dynamic power management device may be used in conjunction with non-volatile semiconductor memories, for example, in which case power to the memories may be substantially or completely turned off except during access. The dynamic power management device may be used to greatest advantage in conjunction with DRAMs, however, because of the requirement of DRAMs for a continuous supply

of power. When used in conjunction with DRAMs, the dynamic power management device supplies power to the memory sufficient to maintain memory information during periods of no data access activity and sufficient to exchange memory information with the memory during periods of data access activity. Hence, during periods of no data access activity, a minimal voltage is supplied to memory. During periods of data access activity, a greater operational voltage is supplied to memory. During transitional periods from non-activity to activity, the voltage is ramped up and then ramped back down. For DRAMs, data access activity includes both memory refresh and memory access.

Furthermore, inputs to memory chips are "driven softly" to conserve power. For capacitive loads, the power consumed is proportional to the time rate of change of voltage, dV/dt. The time rate of change of voltage is also referred to as the slew rate. The dynamic power management device uses slew rate controllers, driver circuits designed to have voltage rise and fall times prolonged in comparison to those of usual driver circuits, in order to reduce the slew rate and hence power consumption. Furthermore, address inputs are encoded using gray code such that only one address input changes at a time. Finally, in order to minimize the power consumed by multiple chips, data is stored into and read out of the chips serially with tens or

even hundreds of consecutive bytes being stored on a single chip, such that only one chip needs to be active at any given time, thus reducing power consumption.

Referring now to Figure 1, the dynamic power management device 10 may be interposed between a host device provided with an intelligent interface, such as an AT/IDE, ESDI or SCSI interface, and the solid state memory 13. Intelligent interfaces such as the IDE, ESDI and SCSI interfaces are typically attached between a host computer and a rotating memory device. The host merely requests blocks of data information in 512-byte increments. The data is then intelligently managed between the rotating memory device and the host system. An error recovery system causes operations resulting in errors to be retried. In this manner, the intelligent interface provides a data path from the mass storage device to the host system without apparent data failure. The power management device may be used in a solid state disk that in comparison to conventional hard disks offers greatly improved performance but looks to the computer exactly like a conventional hard disk.

As seen in Figure 1, the dynamic power management device 10 provides all of the data, address and control inputs for the solid state memory 13. The dynamic power

management device also provides an operating voltage VCC to the solid state memory 13. The voltage VCC is dynamically varied, or "cycled" according to different modes of operation of the solid state memory 13. The data output of the solid state memory 13 is received by the dynamic power management device 10. Preferably, the power management device 10 is realized predominantly as a single integrated circuit. In Figure 1, blocks to the left of the dashed vertical line are preferably realized on a single chip.

The slew rates of all of the digital inputs to the solid state memory 13 are minimized using slew rate controllers 15, 17 and 19 to conserve power. As previously mentioned, the slew rate controllers may be input drivers designed to have prolonged rise times and fall times in comparison to conventional input drivers. Further power conservation is achieved by Gray coding address inputs to the solid state memory 13. A binary address generator 21 generates binary addresses in response to a request from the host or in response to a refresh timer block 23. The refresh timer block 23 implements two different refresh timers, one for regular refresh and one for extended refresh, to take advantage of the extended refresh capabilities of some solid state memories. Extended refresh is much slower, typically ten times slower, than conventional refresh and therefore consumes less power.

Binary addresses generated by the address generator 21 are Gray coded by an encoder 25 before being input to the slew rate controller 17 and to the solid state memory 13.

Power to the solid state memory is controlled using pulse width modulation (PWM) by a PWM rate controller 27. Power is supplied by either a main battery BAT1 or a backup battery BAT2 selected between by a power director 29. Voltages from the main and backup batteries, a select signal from the power director 29 and a pulse width modulation signal from the PWM rate controller 27 are all input to an external low pass filter 31. In an exemplary embodiment, the low pass filter 31 may be a conventional RLC filter and may additionally include a selection circuit and a FET power driver. The selection circuit selects either the main battery, the backup battery, or possibly some other power source to supply power to the FET power driver. The pulse width modulation signal from the PWM rate controller 27 is filtered in the low pass filter and input to the FET power driver, which produces the voltage VCC. The voltage VCC is used to power the solid state memory 13 and is also input to the power director 29.

Closed-loop power monitoring is performed by the power director 29, an A/D converter 33 and a power feedback block 35 under the control of a timing sequencer and

arbitor 37. The power director 29 receives voltages from each of the power sources in addition to the controlled voltage VCC. Preferably the power director 29 also produces an internal reference voltage for calibration purposes. The foregoing voltages are input to an analog multiplexer or other analog switch and are selected in turn by the timing sequencer and arbitor 37 to be sampled using the A/D converter 33. The digital representation of the selected voltage is input to the power feedback block 35, which compares the voltage value with a voltage value required by the solid state memory 13 in a particular mode of operation. The power feedback block 35 notifies the timing sequencer and arbitor 37 whether or not the selected voltage is sufficient for the desired operation. If not, the pulse width duty cycle may be increased or another source may be selected. Closed-loop monitoring ensures that an adequate voltage is applied to the solid state memory 13.

The timing sequencer and arbitor generates all the necessary control signals for the solid state memory 13 including RAS, CAS and WE signals. When power is insufficient, the control signals that initiate an operation are delayed until adequate power has been confirmed. The timing sequencer and arbitor 37 also

arbitrates between memory access by the host and memory refresh.

Data is input to and output from the solid state memory 13 across a data path including an error correction block 39 and a serializer/deserializer 41. Error detection and correction is performed using a well-known polynomial cyclic redundancy code (CRC). Incoming data is therefore error correction coded, serialized in the serializer/deserializer 41 and input to the solid state memory 13 through the slew rate controller 17. Data output from the solid state memory 13 are deserialized in the serializer/deserializer 41 and input to the error correction block 39 for error detection and correction. Error-free data is then transferred to the host on a parallel data bus 43.

Data path control is provided by a DMA controller 45 in cooperation with a data sequencer 47 connected to the timing sequencer and arbitor 37. The DMA controller 45 performs data transfer handshaking with the host. The DMA controller 45 is also provided with byte count registers to keep track of the number of data bytes remaining to be transferred. The data sequencer 47 signals the DMA controller 45 when a data byte is ready to be transferred, whereupon the DMA controller 45 issues a DMA request (DRQ)

to the host. Upon acknowledgement of the request from the host by means of a DMA acknowledge signal (DACK), the byte is transferred on the parallel data bus 43. When all bytes have been transferred, the DMA controller 45 raises a transfer done signal, signaling the host that the requested number of data bytes, for example 512, have been transferred. The data sequencer 47 controls all timing internal to the dynamic power management device 10. The data sequencer 47 therefore controls conversion of data between serial and parallel. The data sequencer also controls operation of the error correction block, 39, supervises direct memory access, and times out the memory control signals RAS, CAS and WE.

The dynamic power management device is also provided with a daisy chain controller 49 allowing multiple dynamic power management devices each associated with one or more solid state memories to be connected together to realize a single high-capacity solid-state memory. The daisy chain controller 49 is provided with a serial input SI and ~~in~~ a serial output signal SO for communication with a daisy chain controller in another dynamic power management device. When data is required to be read from or written to a solid state memory associated with a dynamic power management device (slave) other than the dynamic power management device in communication with the host (master),

the data sequencer 47 causes a command to be daisy chained to the appropriate dynamic power management device. Data provided from another power management device is transferred in serial form from the daisy chain controller 49 to the serializer/deserializer 41 where it is converted to parallel form for transfer to the host. Data from the host to be provided to another dynamic power management device is serialized in the serializer/deserializer 41 and transferred to the daisy chain controller 49 to be passed down the chain to the appropriate dynamic power management device.

Operation of the dynamic power management device 10 to cycle power to the solid state memory 13 in accordance with different modes of operation of the solid state memory may be appreciated from Figures 2a-2d ~~Figure 2~~. During a standby period of operation shown in Figure 2b, the operational voltage supplied to the solid state memory 13, shown in Figure 2a, cycles between approximately 1.5 volts and 2 volts. During this period, the pulse width modulation signal is set to a minimum duty cycle sufficient to maintain data in the solid state memory 13. With each pulse, the voltage rises to approximately 2 volts; between pulses, the low pass filter 31 causes the voltage to be sustained at about 1.5 volts. In preparation for a refresh cycle during a Prepare Refresh period shown in Figure 2b,

the duty cycle of the pulse width modulation signal is increased, causing the voltage to ramp up from about 1.5 volts to about 3 volts. When the voltage has reached about 3 volts, sufficient to perform a refresh operation, the power feedback block 35 of Figure 1 signals the timing sequence and arbiter 37 that it may proceed with a RAS cycle, initiating refresh. During a refresh period shown in Figure 2b, the RAS signal generated by the timing sequencer and arbiter 37 drops low from a nominal value of about 2.7 volts. Current flow increases correspondingly from a quiescent current of about 100 microamps to about 1000 microamps. When refresh has been completed, the RAS signal is again raised, causing the current to drop to the quiescent level. The voltage supplied to the solid state memory is thereafter ramped down during a Prepare Standby period, after which the dynamic power management device 10 resumes standby operation.

Referring now to Figure 3, expansion of the solid state memory from a single solid state memory device to any number of solid state memory devices may be achieved in two different ways. Using the daisy chain capability described in relation to Figure 1, multiple dynamic power modules may be daisy chained together, each constituting a memory node. In addition, the dynamic power module may be modified to provide multiple ports, and a string of multiple memory

devices may be connected to each port. In Figure 3, four ports are provided and four memory devices are connected to each port such that a total of 16 memory devices are controlled by each dynamic power module. Connection of the memory devices to the dynamic power modules has been illustrated in simplified form. Each of the illustrated busses in practice includes data, address and control signals as well as an analog power bus.

The voltage across one of the strings of four memory devices during operation of the dynamic power modules is shown in Figure 4. During refresh, the voltage rises to about 3.3 volts. In between refresh intervals, the voltage pulsates between about 1.5 and 2.5 volts.

The corresponding plot of power consumption is shown in Figure 5. In between refresh intervals, power consumption remains well below 2 milliwatts. Slight power "bumps" occur at approximately 1 microsecond intervals, corresponding to the pulse width modulation rate. During refresh, power consumption spikes up sharply to about 13 milliwatts for a period of time on the order of 100 nanoseconds. Power consumption then subsides and resumes the previous pattern.

A corresponding plot of total battery power consumed over time is shown in Figure 6. The amount of power consumed increases at a rate of about 3 milliwatts per microsecond up until refresh, at which time a step increase in power consumption of about 20 milliwatts occurs, followed again by power consumption at the 3 milliwatt per microsecond rate.

Figure 7 shows the expected life of a 15 milliamp-hour hot standby ~~stand by~~ battery powering 8 DRAMs as a function of time as power is cycled to the DRAMs. During standby, expected battery life varies from a maximum of just less than 60 days to a minimum of slightly more than 20 days. During access, expected battery life drops precipitously to just several days. On the average, using dynamic power management, the battery may be expected to last more than 30 days, ample time under any normal circumstance. When coupled with the dynamic power management device of the present invention, DRAMs therefore provide a high-performance, high-reliability and cost-competitive alternative to small form factor hard disk assemblies.

The dynamic power management device, besides dynamically managing power consumption of the solid state memory, may also be designed to dynamically manage its own

power consumption. Typically, the solid-state memory is accessed only about 10% of the time and operates in refresh and standby modes 90% of the time. The dynamic power management device may therefore sleep 90% of the time during refresh and standby modes. During refresh mode, only a simple counter is required to remain running to preserve refresh activity. The dynamic power management device wakes up upon access by the host. The dynamic power management device sleeps by: turning off all unnecessary logic; stopping all unnecessary clocking; reducing the clock frequency by a factor of 10; shutting off all unnecessary driver transistors to the outside world; waking up when accessed by an external interface request; and automatically readjusting clocks and active circuits. By managing its own power consumption in addition to the power consumption of memory, the dynamic power management device minimizes overall power consumption.

The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as limited to the particular embodiments discussed. Instead, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by workers skilled in the art without departing

from the scope of the present invention as defined by the following claims.